REMARKS

Claims 1-12 are all the claims pending in the application.

35 USC § 112:

The Examiner rejects claims 1 and 3 under 35 U.S.C. 112, second paragraph, as being indefinite. This is because the Examiner asserts that it is not clear what is referred to by the recitation "all of said decoupling capacitor does not overlap said diffusion layer," in claims 1 and 3. As shown in the exemplary, non-limiting embodiment of Figure 1, the decoupling capacitor is formed in the area where the upper electrode 108 overlaps the oxide film layer 112 and the lower electrode 107, such that the actual "decoupling capacitor" does not extend width-wise past the ends of the upper electrode 108. Although the lower electrode 107 has a portion which extends out from the decoupling capacitor, this portion of the electrode 107 does not form part of the decoupling capacitor. In other words, the decoupling capacitor is formed only in the overlapping areas of elements 108, 107 and 112, such that the portion of the lower electrode 107 extending outside of the decoupling capacitor (i.e., extending beyond the width of the upper electrode 108) is not part of the decoupling capacitor.

Claims 1 and 3 are therefore deemed to be definite, such that the rejection under 35 U.S.C. § 112, second paragraph, should be withdrawn.

35 USC § 102:

Claims 1, 3-5, 7 and 9-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Shirley et al. (US patent No. 6,015,729 [hereinafter "Shirley"]).

The Examiner applies Figure 1 of Shirley for disclosing a semiconductor integrated circuit comprising a power supply wiring and a ground wiring. The Examiner relies on elements 24, 26, and 28 to disclose a decoupling capacitor. Element 16 is applied as being a diffusion layer. The Examiner further asserts that the electrode 28 comprises a shield layer and has a portion[1] formed in a plane shape on a semiconductor substrate 10.

First, Applicants clarify the language of claims 1 and 3 by removing the phrase "all of." Claims 1 and 3 also recite that "a plane shaped portion of said shield layer contacts said diffusion layer." Shirley cannot reasonably be interpreted as disclosing this feature. In particular, the applied portion of the electrode 28 that has a plane shape in Shirley does not contact the diffusion layer 16. Instead, the curved portion of the electrode 28 contacts the diffusion layer.

Moreover, Shirley's decoupling capacitor is essentially the same as the "prior art 1" disclosed in the present application (Japanese Patent Applications Laid Open No. 2001-15601). In particular, the decoupling capacitor taught by Shirley is located on an uppermost part of the semiconductor device and the power supply wiring and the ground wiring are connected to the substrate by contacts which penetrate the interlayer insulating films, so that the aspect ratio of the contact part becomes large and the inductance of the contact part is increased (see, for example, page 2, lines 6-19 of the present specification). Further, Shirley's decoupling capacitors are located over diffused n+ regions 16 or 17 or n-well 12 as shown in FIG 1.

[1] The portion referred to by the Examiner is the planar portion of 28 that is parallel to the substrate.

Accordingly, Shirley does not disclose the unique combination of features recited in claims 1 and 3, such that the rejection thereof under 35 U.S.C. § 102(b) should be withdrawn. The rejection of dependent claims 2 and 4-12 should likewise be withdrawn at least by virtue of these claims respectively depending from claims 1 and 3.

35 USC § 103:

Claims 2, 6, 8 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shirley in view of Tobita (US patent No. 5,801,412).

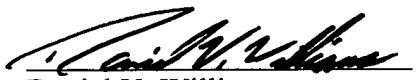
The Examiner acknowledges that Shirley does not explicitly teach or suggest the features of claim 2 regarding a wiring layer connected to wirings on an uppermost layer of a multi-layer wiring structure via contact electrodes, and a capacitor insulating film for forming the decoupling capacitor provided between the wiring layer and the shield layer. Shirley also does not teach that the shield layer comprises a silicon compound of a metal. Therefore, the Examiner relies on Tobita.

Without conceding to the grounds of rejection, Applicants submit that Tobita fails to make up for the deficient teachings of Shirley in regard to claims 1 and 3, such that claims 2, 6, 8 and 11-12 are patentable at least due to their respective dependencies.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



Daniel V. Williams
Registration No. 45,221

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
23373
CUSTOMER NUMBER

Date: July 7, 2006